Appendix A: Pending Claims

1. A method for forming a stacked package of at least an upper semiconductor package unit and a lower semiconductor package unit, the method comprising:

(a) flattening leads of said upper semiconductor package unit;

(b) shortening at least one selected lead of said upper semiconductor package unit such that the shortened said lead does not contact a lead of said lower semiconductor package unit when said upper semiconductor package unit is stacked atop said lower semiconductor package unit in a same orientation;

(c) stacking said upper semiconductor package unit on said lower semiconductor package unit in said same orientation;

(d) forming a direct electrical connection between two leads of said upper semiconductor package unit; and

(e) forming direct electrical connections between leads of said upper semiconductor package units and corresponding leads of said lower semiconductor package unit.

2. The method of claim 1, wherein step (d) includes forming said direct electrical connection by soldering said two leads.

3. The method of claim 1, wherein step (e) includes forming said direct electrical connections by soldering corresponding said leads.

4. The method of claim 1, wherein said upper and lower semiconductor package units have identical lead layouts.

5. The method of claim 1, wherein said upper semiconductor package unit has a chip-select (CS) lead and a not-connected (NC) lead, and wherein step (d) further includes forming a direct electrical connection between said CS lead and said NC lead.

6. The method of claim 5, wherein step (d) includes forming said direct electrical connection by soldering said CS lead and said NC lead.

7. The method of claim 1, wherein said upper semiconductor package unit has a clock-enable (CKE) lead and a not-connected (NC) lead, and wherein step (d) further includes forming a direct electrical connection between said CKE lead and said NC lead.

8. The method of claim 7, wherein step (d) includes forming said direct electrical connection by soldering said CKE lead and said NC lead.

9. The method of claim 1, wherein said upper semiconductor package unit has a chip-select (CE) lead and step (b) further includes shortening a length of said CE lead of said upper semiconductor package unit.

10. The method of claim 1, wherein said upper semiconductor package unit has a clock-enable (CKE) lead and step (b) further includes shortening a length of said CKE lead.

11. The method of claim 1, wherein said upper semiconductor package unit has a chip-select (CS) lead and step (e) excludes selecting said CS lead.

12. The method of claim 1, wherein said upper semiconductor package unit has a clock-enable (CKE) lead and step (e) excludes selecting said CKE lead.